**18CS203J- Computer Organisation and Architecture**

**Easy Questions**

1. Methodology by which performance improved by executing two or more tasks simultaneously is :
2. Collaborative processing
3. Parallel Processing
4. Concurrent Processing
5. Simultaneous processing

Answer: (b)

1. Technique towards reducing the amount of time needed to wait for a particular task to be solved in parallelism is:
2. Increasing computational Speed
3. Increasing performance
4. Increasing throughput
5. Latency reduction

Answer: (a)

1. Technique towards completing number of process or tasks ina given unit of time is
2. Enhancing the throughput
3. Enhancing the process
4. Enhancing Tasks
5. Reduction of processing time

Answer: (a)

1. Type of parallelism where data is distributed across different nodes in parallel are called
2. Instruction level
3. Data Level
4. Task level
5. Transaction level

Answer: (b)

1. Which type of parallelism do not depend on each other for execution ?
2. Instruction level
3. Task Level
4. Transaction Level
5. Data Level

Answer: (a)

1. Data-level parallelism/task-level parallelism in a tightly coupled equipment whichpermits communication among parallel threads, are handled by
2. Instruction-Level Parallelism
3. Request-Level Parallelism
4. Thread-Level Parallelism
5. Vector Architectures and Graphic Processor Units

Answer: (c)

1. The \_\_\_\_\_\_\_\_\_\_\_\_\_do not have parallel processing capabilities
2. Single Instruction stream, Single Data stream
3. Single Instruction stream, Multiple Data stream
4. Multiple Instruction stream, Multiple Data stream
5. All of the above

Answer: (a)

1. Type of computer where a single instruction would operate or execute on multiple data values by sharing common memory is called
2. Single Instruction stream, Multiple Data stream
3. Single Instruction, Single Data Stream
4. Multiple Instruction, Single Data Stream
5. Multiple Instruction, Multiple Data Stream

Answer: (a)

1. Type of threading which switches between threads on each instruction is called
2. Fine Grained
3. Coarse Grained
4. Simultaneous
5. All of above

Answer: (a)

1. Type of machines which got equal access and access times to memory are:
2. Uniform Memory Access (UMA)
3. Cache Coherent UMA
4. Non-Uniform Memory access (NUMA)
5. COMA

Answer: (a)

1. In memory chip, each memory cell can hold how many much of information
2. 1 bit
3. 1 byte
4. 2 Kilo byte
5. 1Mega Byte

Answer: (a)

1. In memory chip, all cells in row are connected to a common line called
2. Word line
3. Control line
4. Read line
5. MUX

Answer: (a)

1. MESI Protocol is a sort of inquisitive \_\_\_\_\_\_\_\_\_\_\_\_
2. Cache protocol
3. Processor protocol
4. Memory protocol
5. Instruction protocol

Answer: (a)

1. In MESI Protocol, \_\_\_\_\_\_\_\_\_\_\_\_\_ state specifies that the cache line is existing in current cache only and its significance is diverse from the main memory.
2. Modified
3. Exclusive
4. Shared
5. Invalid

Answer: (a)

1. In SRAM cell for reading state, Switches T1 and T2 are in
2. Closed state
3. Open
4. Grounded
5. None

Answer: (a)

1. In which mapping, the data can be mapped anywhere in the cache memory?

(a) Associative

(b) Direct

(c) Set Associative

(d) Indirect

Answer: (a)

1. Which of the memory chips are volatile ?
2. SRAM
3. DRAM
4. SRAM and DRAM
5. EPROM

Answer : (c)

1. Which of memory allows the data to be erased and loaded by reprogramming ROM?
2. EPROM
3. PROM
4. EEPROM
5. FLASH

Answer: (a)

1. Cache memory
2. has greater capacity than RAM
3. is faster to access than CPU Registers
4. is permanent storage
5. isfaster to access than RAM

Answer: (d)

1. Type of memory for increasing the size of the memory system is called
2. Virtual Memory
3. Cache Memory
4. L1 Cache
5. L2 Cache

Answer: (a)

**Moderate Questions**

1. The instruction is said to be in\_\_\_\_\_\_\_\_\_\_\_\_\_\_while it is between its start and end of itsrunning phase.

(a). Execution

(b) Wait

(c) Stall

(d) Branching

Answer: (a)

1. Which class of systems belongs to von Neumann computer?

(a). SIMD (Single Instruction Multiple Data)

(b). MIMD (Multiple Instruction Multiple Data)

(c). MISD (Multiple Instruction Single Data)

(d.) SISD (Single Instruction Single Data)

Answer: (d)

1. SIMD symbolizes an organization that.

(a). refers to a computer system capable of processing several programs at the sametime.

(b). represents organization of single computer containing a control unit, processorunit and a memory unit.

(c) Includes many processing units under the supervision of a common controlunit.

(d) None of the above

Answer: (c)

1. Multiple tasks executing independently is called as \_\_\_\_\_\_\_\_\_\_\_

(a). Multithreading

(b). Multiprogramming

(c) . Multitasking

(d.) Synchronization

Answer: (b)

1. Which is the suitable one for increasing processor word size in a parallelism.

(a). Increasing

(b). Count based

(c). Bit based

(d). Bit level

Answer: (d)

1. The cost of a parallel processing can be resolute by

(a). Time Complexity

(b). Switching Complexity

(c) Circuit Complexity

(d). None of the above

Answer: (c)

1. Flynn’s Classification discriminates multi-processor computer structural design rendering to

(a). Independent dimensions of Instruction stream and Data stream

(b). Dependent dimensions of Instruction stream and data stream.

(c). Independent dimensions of memory and processor.

(d). Dependent dimensions of memory and I/O stream.

Answer: (a)

1. A write is only performed liberally in MESI protocol, if the cache line is in

(a). Either Modified or Exclusive state

(b). Modified state only

(c). Shared state or Invalid state

(d). Shard state only

Answer: (a)

1. \_\_\_\_\_\_\_\_\_\_\_\_\_ ensures write back caches.

(a). MOSI protocol

(b) MOESI protocol

(c). MESI protocol

(d) MSI protocol

Answer: (c)

1. \_\_\_\_\_\_\_ is a full cache coherence protocol that encompasses all of the possible states commonly used in other protocols.
2. MOESI protocol
3. MESI protocol
4. MSI protocol
5. MOSI protocol

Answer: (b)

1. When a processor needs to read a block which none of the other processors have and then writeto it, the MESI protocol uses \_\_\_\_\_\_\_\_\_\_\_\_\_.
2. Shared
3. Exclusive
4. Invalid
5. Owned

Answer: (b)

1. A cache line in \_\_\_\_\_\_\_\_ state does not hold a valid copy of data with respect to MESI protocol.

(a). Shared

(b). Exclusive

(c). Invalid

(d). Owned

Answer: (c)

1. Which cache write mechanism allows an updated memory location in the cache to remain out of date in memory until the block containing the updated memory location is replaced in the cache?
2. Write through
3. Write back
4. Both write through and write back
5. Cycle Stealing

Answer: (b)

1. Assume the data bus width of DDR memory system is 32 bits. How many cycles does it take to transfer 64B cache block?
2. 64
3. 16
4. 8
5. 1

Answer: (c)

1. The Translation Look Aside Buffer (TLB) stores
2. Branching data
3. Map of Cache data and RAM data
4. Map of Physical Address and Logical Address
5. Memory Translation times

Answer: (b)

1. Page fault occurs when
2. requested page is in memory
3. a requested page is not in memory
4. a page is corrupted
5. None of the above

Answer: (b)

1. Of the following, which best characterizes computers that use memory-mapped I/O?
2. The computer provides special instructions for manipulating I/O ports.
3. I/O ports are placed at addresses on the bus and are accessed just like other memorylocations.
4. To perform an I/O operation, it is sufficient to place the data in an address register and call thechannel to perform the operation.
5. Ports are referenced only by memory-mapped instructions of the computer and are located athardwired memory locations.

Answer: (b)

1. In dynamic memory chip, technique for reducing the number of pins are:
2. Multiplexing addresses
3. Reducing address lines
4. Address Decoder
5. Encoder

Answer: (a)

1. FromAmong the following, which has biggestlargest memory size ?
2. Registers
3. Magnetic Disk
4. Memory
5. Cache

Answer: (b)

1. Techniques for improving hit rate are :
2. Increasing block size
3. Increasing block size with constant cache size
4. Increasing cache memory
5. Increasing main memory

Answer: (b)

1. Process of bringing the data before Read miss occurs is
2. Prefetching
3. Fetching
4. Executing
5. Read hit

Answer: (a)

1. Which among the following is true?
2. The memory allocated to each page is contiguous.
3. The offset is different in a virtual address and a physical address
4. Logical address space can be smaller than physical address space\
5. Segmentation avoids external memory fragmentation

Answer: (a)

1. The starting address of a page table in kept in

(a) Main Memory

(b) Cache Memory

(c) Register

(d) Page Table Base Register

Answer: (d)

1. Memory management technique in which system stores and retrieves data from secondary storage foruse in main memory is called
2. Fragmentation
3. Paging
4. Mapping
5. Indexing

Answer: (b)

1. Which of following refers to programme Controlled I/O
2. JMP
3. BR
4. CMP
5. All of Above

Answer: (d)

Difficult

1. Consider an instruction as follows:

A= (L1\*L2) + (L3\*L4)

B= (L1\*L2) - (L3\*L4)

So for this compute the software and hardware parallelism and show diagrammatically cycles.//Question is unclear. How to show diagrammatically?

1. 2.67 and 1.14
2. 2.67 and 1.0
3. 2.5 and 1.14
4. 2.55 and 1.14

Answer: (a)

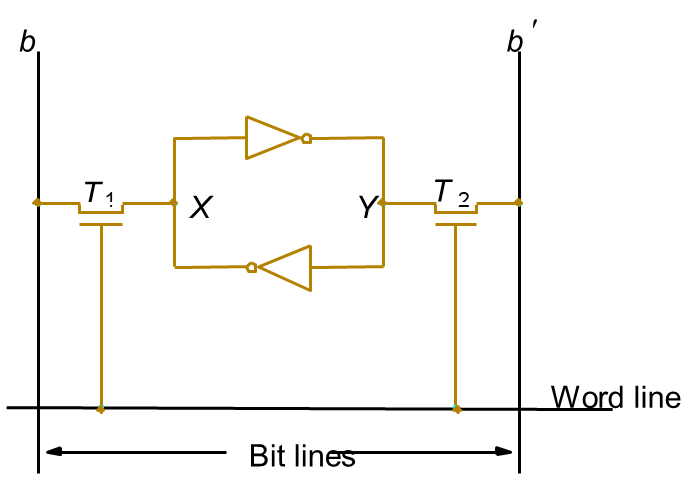
1. Let us assume we want to sum all the elements of the given array of size 10 and the time for a single addition operation is 2 time units. If we execute this job as a data parallel job on 4 processors the time taken would reduce be what ? Assuming merging overhead time unit is 5 time units
2. 10 time units
3. 5 time units
4. 15 time units
5. 7 time units

Answer: (a)

1. Consider a 4 core processor named as Core 1, Core 2, Core 3, and Core 4. Main memory is holding data say X= 1500H. Core 1 reads value of X which is 1500H. Core 2 also read same value of X which is 1500H. Core 1 writes to X which is 3000 H. Core 2 attempts to read X which is old copy i.e 1500H. What kind of problem it is and solution to it is
2. Cache Coherence and invalidation is done where copies of X in other caches are invalidated.
3. Cache miss
4. Cache coherence and snooping done to monitor the bus connecting cores
5. (a) or (c)

Answer: (d)

1. Consider the circuit given below. For read operation, what should be done



1. Switches T1 and T2 are grounded
2. Switch T1 and T2 are closed by activating the word line
3. Sense/Write circuits monitor the status of b and b’
4. (b) and (c)

Answer: (d)

1. Consider a situation where device requesting for service by sending a special code to processor. Based on code, device identified by the processor and interrupt here produces call to predetermined memory location , which is starting address of ISR. Such interrupts refer to what.
2. Polling
3. Priority interrupt
4. Vectored Interrupt
5. All of Above

Answer: (c)